

IN THE CLAIMS

What is claimed is:

- 1 **1.** A noise level detecting circuit, comprising:
2 a pedestal level detecting circuit coupled to receive a digital video
3 signal and providing a pedestal level signal; and
4 an absolute value circuit coupled to receive the pedestal level signal
5 and providing a positive pole component burst signal.

- 1 **2.** The noise level detecting circuit of claim 1, further including:
2 an analog to digital converter coupled to receive an analog video
3 signal and providing the digital video signal.

- 1 **3.** The noise level detecting circuit of claim 1, further including:
2 a timing generating circuit coupled to receive a horizontal synchronous
3 signal and providing a burst gate pulse; and
4 an AND circuit coupled to receive the digital video signal and the
5 burst gate pulse and providing an extracted burst signal.

- 1 **4.** The noise level detecting circuit of claim 1, further including:
2 a delay circuit coupled to receive the positive pole component burst
3 signal and provide a delayed signal.

- 1 **5.** The noise level detecting circuit of claim 4, further including:
- 2 a comparator coupled to receive the positive pole component burst
- 3 signal and the delayed signal and providing a noise level detecting signal.
- 1 **6.** The noise level detecting circuit of claim 5, wherein:
- 2 the delayed circuit delays the positive pole component burst signal by
- 3 one horizontal scanning unit to provide the delayed signal.
- 1 **7.** The noise level detecting circuit of claim 5, further including:
- 2 a line integrating circuit coupled to receive the noise level detecting
- 3 signal and providing a line integrated noise level detection signal.
- 1 **8.** The noise level detecting circuit of claim 7, further including:
- 2 a field integrating circuit coupled to receive the line integrated noise
- 3 level detection signal and providing a field integrated noise level detection
- 4 signal.
- 1 **9.** A noise level detecting circuit, comprising:
- 2 a pedestal level detecting circuit coupled to receive a digital video
- 3 signal and providing a pedestal level signal; and
- 4 an absolute value circuit coupled to receive the pedestal level signal
- 5 and an extracted burst signal and providing a positive pole component burst
- 6 signal;

7 wherein the pedestal level detecting circuit detects a pedestal level of
8 the digital video signal and the absolute value circuit converts the extracted
9 burst signal into the positive pole component burst signal.

1 **10.** The noise level detecting circuit of claim 9, further including:

2 an analog to digital converter coupled to receive an analog video
3 signal and providing the digital video signal wherein the analog to digital
4 converter converts the analog video signal into the digital video signal.

1 **11.** The noise level detecting circuit of claim 10, further including:

2 a timing generating circuit coupled to receive a horizontal synchronous
3 signal and providing a burst gate pulse; and

4 an AND circuit coupled to receive the digital video signal and the
5 burst gate pulse and providing the extracted burst signal;

6 wherein the timing generating circuit generates the burst gate pulse for
7 extracting a burst signal during a period where the burst signal exists in a
8 horizontal blanking period and the AND circuit extracts the burst signal from
9 the digital video signal when the burst gate pulse is provided.

1 **12.** The noise level detecting circuit of claim 9, further including:

2 a delay circuit coupled to receive the positive pole component burst
3 signal and provide a delayed signal.

1 **13.** The noise level detecting circuit of claim 12, wherein:

2 the delay circuit delays the positive pole component burst signal by
3 one horizontal scanning unit to provide the delayed signal.

1 **14.** The noise level detecting circuit claim 12, further including:

2 a comparator coupled to receive the positive pole component burst
3 signal and the delayed signal and providing a noise level detecting signal

4 wherein the comparator compares the positive pole component burst
5 signal with the delayed signal to provide a noise level detecting signal.

1 **15.** The noise level detecting circuit of claim 14, further including:

2 a line integrating circuit coupled to receive the noise level detecting
3 signal and providing a line integrated noise level detection signal.

1 **16.** The noise level detecting circuit of claim 15, wherein:

2 the line integrating circuit integrates signal comparison information
3 from the comparator by a given scanning line period.

1 **17.** The noise level detecting circuit of claim 15, further including:

2 a field integrating circuit coupled to receive the line integrated noise
3 level detection signal and providing a field integrated noise level detection
4 signal.

1 **18.** The noise level detecting circuit of claim 17, wherein:

2 the line integrating circuit integrates signal comparison information
3 from the comparator by a given scanning line period and the field integrating
4 circuit integrates the signal comparison information after the line integration
5 by a given field period.

1 **19.** A noise level detecting circuit, comprising:

2 an analog to digital converter that converts an analog video signal into
3 a digital video signal;

4 a pedestal level detecting circuit that detects a pedestal level of the
5 digital video signal;

6 a timing generating circuit that generates a burst gate pulse for
7 extracting a burst signal during a period where the burst signal exists in a
8 horizontal blanking period;

9 an AND circuit that extracts the burst signal from the digital video
10 signal in a period of the burst gate pulse;

11 an absolute value circuit that converts the burst signal to a positive
12 component burst signal with respect to the pedestal level;

13 a delay circuit that delays the positive component burst signal; and

14 a comparator that compares one positive component burst signal with
15 another positive component burst signal delayed by the delay circuit.

1 **20.** The noise level detecting circuit of claim 19, further including:

2 a line integrating circuit that integrates signal comparison information
3 from the comparator by a predetermined scanning line period; and
4 a field integrating circuit that integrates information after the line
5 integration by a predetermined field period.